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TITLE: Digital video horizontal synchronization pulse detector and processor

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Referring to FIG. 3, a detailed schematic block diagram of the sync position error circuit 32 is shown. The sync position error circuit 32 includes a 4-bit counter 122, a 4-bit digital **decoder** 124 and an AND gate 126. The 4-bit digital counter 122 counts between -8 and +7 when the window pulse 36 is high and the counter 122 has not counted to its maximum value of +7, as shown in FIGS. 7-10. When the window pulse 36 is high, and the value of the counter 122 has not reached +7, the two inputs to the AND gate 126 are high causing the AND gate 126 to output a digital high to a count enable input 128 of the 4-bit digital counter 122. During this time, the counter 122 which is clocked by the reference clock 22, outputs a 4-bit digital data stream which increments up in binary numbers from -8 to +7 under 2's

complement arithmetic which is used throughout the digital video horizontal synchronization pulse detector and processor 10.

This 4-bit digital data stream is applied to the **decoder** 124 which decodes the 4-bit digital data and outputs a low output when the count equals +7. When this occurs, the output from the AND gate 126 goes low which subsequently disables the counter 122 from further counting. In addition to applying the 4-bit digital data stream to the **decoder** 124, the 4-bit digital data stream is also applied to a 4-bit latch 130. The 4-bit latch 130 latches the value of the counter 122 upon receiving the external horizontal sync pulse 30 from the horizontal sync detection circuit 24. The digital value in the latch 130 represents the error of the rising edge of the external horizontal sync pulse 30 with respect to the center of the window pulse 36, as seen in FIG. 7, when the external horizontal sync pulse 30 occurs within the window pulse 36. If the external horizontal sync pulse 30 does not occur within the window pulse 36, the error is limited to the maximum value of +7, to provide noise immunity to the horizontal sync detector and processor 10. This error is outputted from the error output 40 and received by the error input 56 of the long term

averaging circuit 58.

Referring to FIG. 4, a detailed schematic block diagram of the acquisition circuit 44 is shown. The acquisition circuit 44 includes an AND gate 138, a 5-bit D-Q digital counter 140, a 5-bit **decoder** 142 and a digital register 144. The counter 140 counts up when the out-of-range output 42 is low and counts down when the out-of-range output 42 is high. The counter 140 is incremented up or down on each H-state update pulse 52, after an external horizontal sync pulse 30 is generated. The 5-bit digital data stream from the counter 140 is applied to the digital **decoder** 142 which outputs a digital high output at count equals 0 and a digital high output at count equals 31.

At count equals 0, the digital high output is applied to the AND gate 138 such that if the out-of-range output 42 is high, indicating the counter should count down on the next H-state pulse 52, the two high inputs to the AND gate 138 generate a high output which inhibits the counter 140 from counting below zero (0). Upon reaching the count equal 31, the **decoder** 142 applies a digital high output to the digital register 144. Upon receipt of the next H-state update pulse 52, the digital register 144 outputs the digital high output to the

acquire input 46, which places the horizontal counter 48 in the "acquire" mode.
It should be noted that since the counter 140 is a 5-bit counter, it rolls over to a value of zero (0) after the count 31, therefore no resetting of the counter 140 is required.

The 10-bit digital data stream output from the counter 146 is applied to a 10-bit digital **decoder** 160 which decodes the 10-bit digital data stream and outputs digital high outputs at various counts. The **decoder** 160 outputs the window pulse 36 during counts 22 to 37. A reset error pulse 162 occurs at count 800 which is used to reset the 4-bit counter 122 and the latch 132 in the sync position error circuit 32. At count 909, a high input is applied to the reset input 152 to reset the counter 146 to 0 so that the counter continuously counts between 0 and 909. A processed H-sync 163 is generated during counts 27 to 75 which represents the regenerated digital representation of the horizontal sync pulse 16. The H-state update 52 occurs at count 50 which is used by the counter 146 during the "track" mode, as well as to increment the 5-bit counter 140 in the acquisition circuit 44.

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In many of the digital video products in use today, the horizontal synchronization pulse from the analog video signal is regenerated in a clean digital format and used for the horizontal line synchronization of the image, in addition to generating a horizontal sync memory map of the digitized analog video signal. During memory mapping each pixel of the digitized analog video signal is generally stored in X and Y addresses in the digital memory with the horizontal sync pulse used to **reset** the X addresses and the vertical sync pulse used to **reset** the Y addresses. In addition, the regenerated horizontal sync pulse can also be used for timing information in on-screen display circuitry.

The sync position error circuit 32 receives the external horizontal sync pulse

30 at a HSYNC input 34. If the external horizontal sync pulse 30 is within a window pulse 36 received at a window input 38 (FIGS. 7-10), the rising edge position of the external horizontal sync pulse 30 is measured relative to a certain count in an internal counter, details of which will be discussed hereinafter. This counter which is **reset from a reset** error pulse 162 generates a positive or negative time position error value if the rising edge of the external horizontal sync pulse 30 is not centered within the window pulse 36. This error value is output from an error output 40. If the external horizontal sync pulse 30 is not within the window pulse 36, a 1-bit out-of-range output 42 goes low (i.e. digital logic "0") which is applied to an acquisition circuit 44. In addition, the time position error value is also limited to a maximum error value because of the window pulse 36.

The digital output of the acquisition circuit 44 is applied to an acquire input 46 of a local horizontal counter 48. The local horizontal counter 48 essentially acts as a saw-tooth oscillator which is phase-locked to the external horizontal sync pulse 30. The horizontal counter 48 is clocked by the reference clock 22 and has a period equal to the period of a single horizontal

line in the video signal 14. That is, in NTSC format, the horizontal counter 48 will count from 0 to 909 and then **reset** to 0 and count again to 909 continuously since there are 910 samples or pixels in each horizontal scanning line.

The sync position error circuit 32 also includes a 1-bit latch 132 which latches the window pulse 36 upon receipt of the external horizontal sync pulse 30. If the external horizontal sync pulse 30 occurs when the window pulse 36 is high, the latch 132 latches a 1-bit digital high output to the out-of-range output 42 which indicates that the external sync pulse occurred during the window pulse 36, as shown by the out-of-range output 42 in FIG. 7. If the window pulse 36 is low when the external horizontal sync pulse 30 occurs, the latch 132 latches a 1-bit digital low output at the out-of-range output 42, shown in FIG. 9, which indicates that the external horizontal sync pulse 30 did not occur during the window pulse 36. After each external horizontal sync pulse 30 occurs, the 4-bit counter 122 and the latch 132 are **reset** from the horizontal counter 48 with a **reset** error pulse 162. This **reset** error pulse 162 is applied to a **reset** input 134 of the 4-bit counter 122 and a **reset** input 136 of the latch 132.

At count equals 0, the digital high output is applied to the AND gate 138 such that if the out-of-range output 42 is high, indicating the counter should count down on the next H-state pulse 52, the two high inputs to the AND gate 138 generate a high output which inhibits the counter 140 from counting below zero (0). Upon reaching the count equal 31, the decoder 142 applies a digital high output to the digital register 144. Upon receipt of the next H-state update pulse 52, the digital register 144 outputs the digital high output to the acquire input 46, which places the horizontal counter 48 in the "acquire" mode.
It should be noted that since the counter 140 is a 5-bit counter, it rolls over to a value of zero (0) after the count 31, therefore no **resetting** of the counter 140 is required.

Referring to FIG. 5, a detailed schematic block diagram of the horizontal counter 48 and the window generating circuit 54 is shown. This circuit includes a 10-bit digital counter 146 which counts up from 0 to 909 in increments of 1 at each reference clock pulse 22, seen in FIGS. 8 and 10. The counter 146 includes a load input 148, a load control input 150 and a **reset** 152. When the load control input 150

receives a digital high, the 10-bit digital value at the load input 148 is loaded into the counter 146 which immediately puts the counter 146 at that count value. The value at the load input 148 is determined by a 10-bit 2-to-1 multiplexer 152 which is controlled by the acquire input 46. The load control input 150 is controlled by a 1-bit 2-to-1 multiplexer 156 which is also controlled or selected by the acquire input 46.

The 10-bit digital data stream output from the counter 146 is applied to a 10-bit digital decoder 160 which decodes the 10-bit digital data stream and outputs digital high outputs at various counts. The decoder 160 outputs the window pulse 36 during counts 22 to 37. A **reset** error pulse 162 occurs at count 800 which is used to **reset** the 4-bit counter 122 and the latch 132 in the sync position error circuit 32. At count 909, a high input is applied to the **reset** input 152 to **reset** the counter 146 to 0 so that the counter continuously counts between 0 and 909. A processed H-sync 163 is generated during counts 27 to 75 which represents the regenerated digital representation of the horizontal sync pulse 16. The H-state update 52 occurs at count 50 which is used by the counter 146 during the "track" mode, as well as to increment the 5-bit counter

140 in the acquisition circuit 44.

If the acquisition circuit 44 accumulates its maximum predetermined value of 31, thereby generating a high output, this high output is applied to the acquire input 62 of the long term averaging circuit 58 which is applied to an AND gate 184. During the next external horizontal sync pulse 30, which is also applied to the AND gate 184, the 15-bit register 172 is **reset** or cleared, via the AND gate 184, so that a new average error can be accumulated. This assures a more accurate average error and further noise immunity.

Referring to FIGS. 8 and 10, the operation of the horizontal synchronization pulse detector and processor 10 is shown in a track mode and an acquisition mode as discussed above. Referring specifically to FIG. 8, the operation of the horizontal sync detector and processor 10 in the track mode is shown. FIG. 8 shows the video signal 14 and how the horizontal counter 48 counts with respect to the video signal 14 to produce the external horizontal sync pulse 30 within the window pulse 36. In addition, FIG. 8 shows the output of the 4-bit counter 122 of the sync position error circuit 32 which counts from -8 to +7 during the window pulse 36 and is **reset by the reset** error 162 from the

horizontal counter 48 at count 800.